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Circuit Level Design Approaches for Radiation-Hard Digital Electronics

C P Jain[1], K.B Joshi[2]

Abstract— In this paper, we present design based architectural techniques for radiation hardened digital electronics. These techniques can be applied at many levels of the design without any changes in the fabrication process technology. These are planned to just detect the presence of an upset in the system or although these are more complex to detect and correct the system error in the presence of an upset. Design based techniques are composed of some kind of redundancy which can be provided by extra components (hardware redundancy) or by an extra execution time or by different instants of data sampling (time redundancy), very often techniques implement a combination of both. We present a Triple Modular Redundancy (TMR) and Code word state preserving technique that ensure radiation tolerance.

Keywords— Design, radiation-hard, reliability, single event upsets (SEUs), soft errors, Radiation Harden By Design (RHBD), Rad-Hard Digital Electronics.

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1 Introduction

Plenty of work has been done on radiation hardened circuit design approaches. These approaches can be classified as device level, circuit level and system level [1]. The device level approaches involve a fundamental change or enhancement of the fabrication process to improve the radiation immunity of a design [2]. Circuit level hardening approaches use special circuit design techniques that reduce the vulnerability of a circuit to radiation dose [3], [4]. The device and circuit level approaches are typically fault avoidance approaches while system level approaches typically involve the use of fault detection and tolerance mechanisms. Triple Modular Redundancy (TMR) is a classical example of a system level design approach [5].

The design level solution is very attractive because it uses a standard CMOS process. However, this solution is specific to the circuit, such as a micro-controller or an ASIC can have different design techniques to avoid SEU and the design engineer is responsible to project the hardened circuit according to its architecture and application. Representative techniques of SEU mitigation at design level solutions are TMR [5].

All design-based techniques are composed of some kind of redundancy which can be provided by extra components i.e. hardware redundancy or by an extra execution time or by different instants of data sampling or time redundancy. Hardware redundancy is basically based on logic redundancy which is characterized as extra components or extra paths that allow the design to continue operation even when some parts fail. Error detection and correction codes (EDAC) can also be seen as a hardware redundancy because it generates redundant bits to be able to detect and correct upsets [6].

Each technique has some advantages and drawbacks, and there is always an optimization in area, performance, power dissipation and fault tolerance efficiency [5], [7] to design a circuit.

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Here, we propose design based mitigation techniques Triple Modular Redundancy (TMR) and Code word state preserving techniques for radiation hard digital circuits.

2. SYSTEM LEVEL DESIGN APPROACHES

2.1. Triple Modular Redundancy

This technique consists of triplicating elements in such a way that the logic value resulting from at least two elements are propagated. This can be used to prevent an error as result of a single fault occurring inside the elements .On the other hand when a single event transient occurs before inputs the transient pulse may be captured by the flip flops.TMR technique can be used in such way that the fault is propagated to only one flip flop by inserting temporal redundancy. There are two implementation of the TMR technique, in the first implementation the clock signal of each flip flop is delayed in such a way that the input signal is captured at three different moments, thus a transient fault at the input is captured only by one of the flip flops and in the other the input signal is delayed by the delay block [5], [7].

A triplicate voting system compares the outputs of three identical devices bit by bit relying on the fact that while each bit is equally vulnerable to upset and the probability of the same bit upsetting in two independent devices is very low. Even a worst case SEFI can only corrupt all the bits on a single chip and so is correctable by triplicate voting and the probability of two SEFIs is negligibly small. The downside of triplicate voting is that it involves over 200% overhead and for large data words, voting each bit can lead to very complicated voting circuitry.

The most common example of TMR is a D-type flip-flop that has been triplicate and to which a voter has to be added on its output. By replacing all flip-flops in design with the circuit shown in fig. 1 one would protect the design against SEUs in the flip-flops. However, this would not protect against SEUs

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in the combinatorial logic connecting the flip-flops in the design [3], [5], [7].

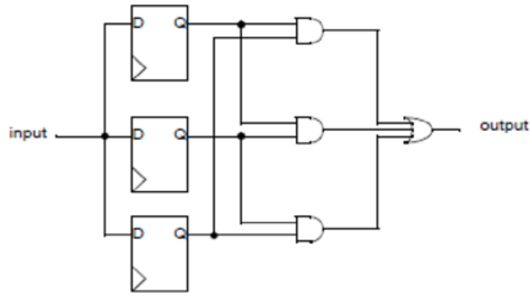

Figure 1 Triple Modular Redundancy with voting.

2.1.1 Radiation Tolerance using Static Triple Modulo Redundancy (TMR)

TMR is an approach where three identical circuits are used for each logic operation. The outputs of the three identical logic circuits are fed into a voting system which produces an output based on the majority of values. This technique assumes that a radiation particle will only strike the diffusion region of one of the circuits creating an SEU. Since the other two circuits in this approach are unaffected, the voting system will disregard the inconsistent result of the effected circuit and produce the correct output [5].

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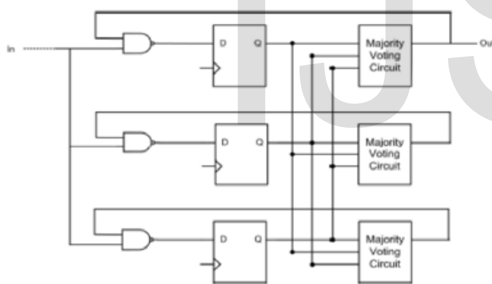

Figure 2 Example Circuit with Radiation Tolerance using Static Triple Modulo Redundancy (TMR).

The drawback of this approach is the increased area and power consumption associated with having three redundant circuits and the additional voting hardware, while the increase in the area is not necessarily a problem due to the high density of modern processes. The power consumption of extra circuitry is a detrimental issue to satellite and mission spacecraft running on portable power cells [7].

2.2. Code word state preserving technique (CWSP)

Radiation strikes cause charge to be dumped on a diffusion node which results in voltage glitches on these nodes. We are concerned with those glitches that cause nodes to change their logical value i.e. those that cross the switch-point of the gate in question and can be captured in a latch or flip-flop thereby leading to incorrect circuit operation [6].

Our approach uses CWSP elements to achieve 100% SET tolerance. In case of a SET event, the correct value is always computed by the CWSP element which is connected in a secondary path, off the functional circuit critical paths. This correct value is used to repeat the computation in case of a SET event, by introducing a bubble in the computation

For a k input gate, the CWSP element has 2k inputs. One set of k inputs are connected to the inputs of the gate that the CWSP element replaces. The other set of k inputs are connected to the delayed version by a delay value d of the first set of k inputs. The CWSP element tolerates glitches of width up to d. In Fig 2, the inputs a and b are the undelayed inputs, while the inputs a^* and b^* are delayed versions of a and b respectively (delayed by d time units). Consider the CWSP element of either the INVERTER or the NAND2 gate. When the input a = a*, and b = b*, each CWSP element behaves normally, and the outputs are resistively driven to not (a) and not (ab) for the INVERTER and the NAND2 gate respectively. However, whenever there is an SET event which results in a glitch on any input, the gate stops driving the output resistively since both the pull up and pull down paths are disabled. At this point the output is held to its last correct value [6].

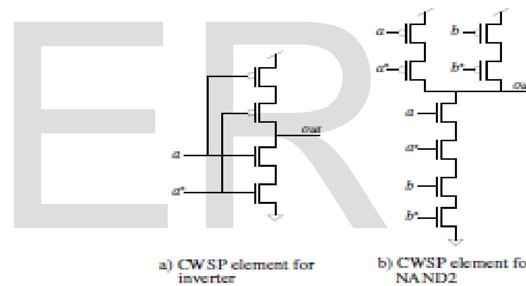

Figure 3 Radiation hardened inverter (a) and NAND gate (b).

3. RESULTS AND CONCLUSION

In order to implement various design techniques, we used the T-SPICE and simulations were done. All basic logic gates were designed by triple modular redundancy and code word state preserving technique and results are reported.

3.1. Triple Modular Redundancy

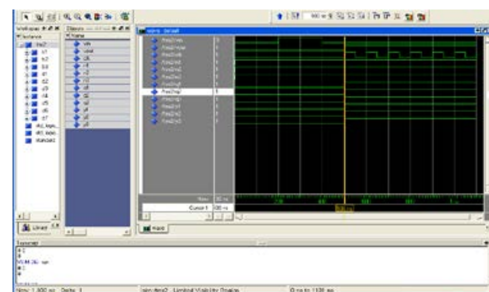

Figure 4 Triple Modular Redundancy.

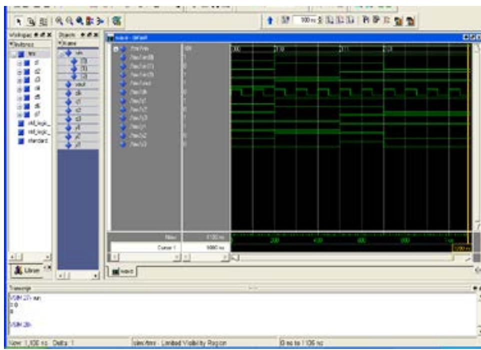

Figure 5 Triple Modular Redundancy with voting.

3.2 Code Word State Preserving Technique

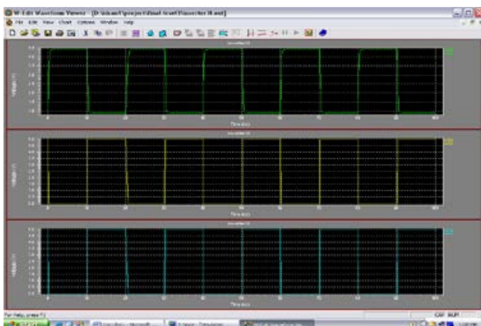

Figure 6 (a) Transient Analysis of radiation Hardened Inverter.

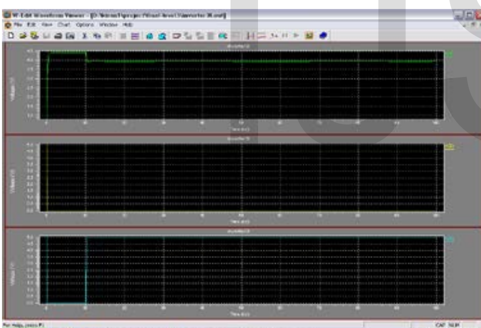

Figure 6 (b) Transient Analysis of radiation Hardened Inverter with state preserving.

3.2.1 NAND GATE

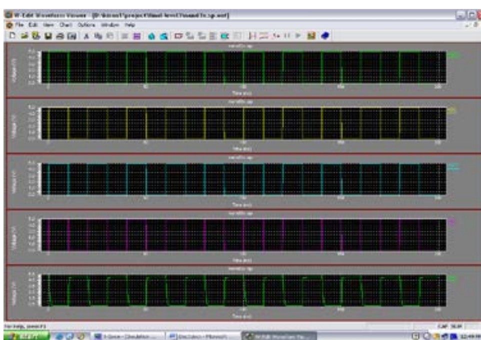

Figure 7 Transient Analysis of radiation Hardened NAND Gate by CWSP.

3.2.2 D-Flip Flop & R S flip flop

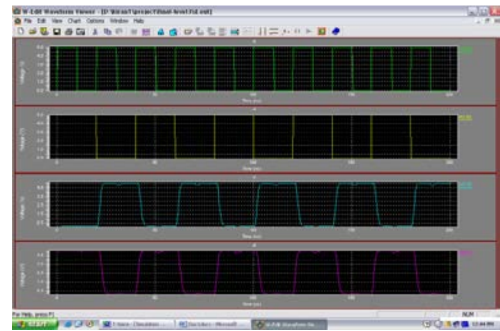

Figure 8 Transient Analysis of radiation Hardened D-FLIPFLOP by CWSP.

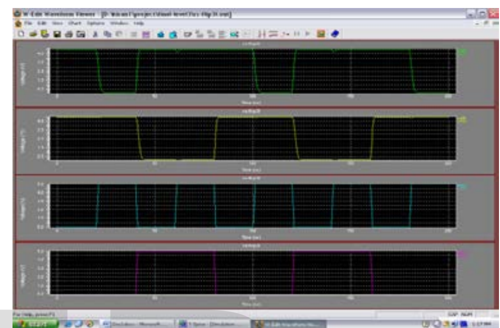

Figure 9 Transient Analysis of radiation Hardened R-S FLIPFLOP by CWSP.

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